A substantially transparent layer **25** overlies the first sections **22**, second sections **23**, and dummy topography **24**. Such transparent layer can comprise silicon dioxide derived from TEOS by LPCVD or derived from silane by LPCVD. Transparent layer **25** can be part of the thick oxide layer deposited as trench fill after shallow trenches are formed during shallow trench isolation (STI) processing. Subsequent to deposition of transparent layer **25**, planarization is effected, as by CMP.

First trenches **23***a* and first uprights **23***b* have approximately the same width w_1, which is strategically chosen such that, when transparent layer **25** is planarized, local imperfections above the global alignment marks, such as "dips" or steps at the edges of active areas **22**, which would cause distortion, are minimized or substantially eliminated. The width w_1 is preferably about equal to the minimum trench width permitted by the design rule of the semiconductor device; for example, about 0.375 μm.

Likewise, the second trenches **24***a* and second uprights **24***b* preferably have approximately the same width w_2 such that, when transparent layer **25** is planarized, local imperfections in planarity are minimized at the outer peripheral edges of the global alignment marks. The width w_2 is preferably about equal to the minimum trench width permitted by the design rule of the semiconductor device; for example, about 0.375 μm. Furthermore, dummy topographical area **24** extends away from the global alignment marks a distance Q such that local variations in planarity of transparent layer **25** caused by the discontinuance of dummy topographical area **24** occur well away from the global alignment marks.

Thus, by providing a segmented section and a peripheral dummy topographical area, local planarization of the transparent material is enhanced, thereby minimizing distortion of the marks' signal and enabling deposition of subsequent layers with substantially planar upper surfaces and minimal degradation of the signal. Although the above-described embodiment of the present invention provides both a segmented section and a peripheral dummy topographical area, either the segmented section or the peripheral dummy area may be employed alone as needed to achieve adequate planarization of the transparent layer above the alignment marks.

The present invention is applicable to the manufacture of various types of semiconductor devices having global alignment marks for use by a stepper, particularly high density semiconductor devices having a design rule of about 0.25μ and under.

The present invention can be practiced by employing conventional materials, methodology and equipment. Accordingly, the details of such materials, equipment and methodology are not set forth herein in detail. In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, as one having ordinary skill in the art would recognize, the present invention can be practiced without resorting to the details specifically set forth. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the present invention.

Only the preferred embodiment of the invention and but a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.

What is claimed is:

1. A semiconductor device, comprising:

a set of alignment marks on a main surface of a semiconductor substrate, the set of alignment marks comprising:

a plurality of active areas each having an upper surface substantially flush with the main surface; and

second sections separating the plurality of active areas such that the active areas and second sections cooperate to produce an interference fringe when illuminated, each second section comprising a plurality of first trenches spaced apart by first uprights having an upper surface substantially flush with the main surface, the first uprights disposed remotely from the active areas; and

a substantially transparent layer having a substantially planar upper surface formed on the set of alignment marks.

2. The semiconductor device as claimed in claim **1**, wherein adjacent active areas and second sections are substantially parallel or substantially orthogonal to each other.

3. The semiconductor device as claimed in claim **2**, wherein the second sections are substantially rectangular.

4. The semiconductor device as claimed in claim **3**, wherein adjacent first trenches and first uprights are substantially parallel or substantially orthogonal to each other.

5. The semiconductor device as claimed in claim **4**, wherein the first trenches are substantially rectangular.

6. The semiconductor device as claimed in claim **1**, comprising a dummy topography area, on the main surface peripheral to the set of alignment marks, comprising a plurality of second trenches spaced apart by second uprights having an upper surface substantially flush with the main surface, the dummy topography area extending a predetermined distance away from the set of alignment marks, wherein the substantially transparent layer extends onto the dummy topography area.

7. The semiconductor device as claimed in claim **6**, wherein adjacent second trenches and second uprights are substantially parallel or substantially orthogonal to each other.

8. The semiconductor device as claimed in claim **7**, wherein the second trenches are substantially rectangular.

9. The semiconductor device as claimed in claim **8**, wherein the first trenches have a first length, and the second trenches have a second length substantially different from the first length.

10. The semiconductor device as claimed in claim **1**, wherein the first trenches and first uprights have approximately the same width.

11. The semiconductor device as claimed in claim **10**, wherein the width of the first trenches and first uprights is about equal to the minimum width according to the design rule for the semiconductor device.

12. The semiconductor device as claimed in claim **10**, wherein the width of the first trenches and first uprights is about 0.3751 μm.

13. The semiconductor device as claimed in claim **6**, wherein the second trenches and second uprights have approximately the same width.

14. The semiconductor device as claimed in claim **13**, wherein the width of the second trenches and second uprights is about equal to the minimum width according to the design rule for the semiconductor device.

15. The semiconductor device as claimed in claim **13**, wherein the width of the second trenches and second uprights is about 0.375 μm.